CLAIMS

[c1] (previously presented) 1. A method for forming an interconnect structure in a magnetic random access memory (MRAM) device, the method comprising:

defining a magnetic stack layer on a lower metallization level, said magnetic stack layer including a non-ferromagnetic layer disposed between a pair of ferromagnetic layers;

defining a conductive hardmask over said magnetic stack layer; and

removing selected portions of said hardmask and said magnetic stack layer, thereby creating an array of magnetic tunnel junction (MTJ) stacks, said MTJ stacks including remaining portions of said magnetic stack layer and said hardmask;

wherein said hardmask forms a self aligning contact between said magnetic stack layer and an upper metallization level subsequently formed above said MTJ stacks.

[c2] (previously presented) 2. The method of claim 1, further comprising:

depositing a cap layer over said MTJ stacks and exposed portions of said lower metallization level;

depositing an interlevel dielectric (ILD) layer over said cap layer; and

defining openings for said upper metallization level in said ILD layer;

wherein portions of said cap layer atop said MTJ stacks are used as an etch stop.

[c3] (previously presented) 3. The method of claim 2, further comprising:

defining via openings in said ILD layer, wherein portions of said cap layer atop said lower metallization level are used as an etch stop.

[c4] (previously presented) 4. The method of claim 3, further comprising:

removing portions of said cap layer exposed by said upper metallization openings and said via openings; and

filling said upper metallization openings and said via openings with a

conductive material by dual damascene processing.

[c5] (previously presented) 5. The method of claim 1, wherein said hardmask comprises a conductive material selected from the group of: tantalum, tungsten, titanium, tantalum nitride, tungsten nitride, titanium nitride, and combinations comprising at least one of the foregoing.

[c6] (previously presented) 6. The method of claim 2, wherein said cap layer comprises silicon nitride.

[c7] (previously presented) 7. The method of claim 1, further comprising:

depositing a cap layer over said MTJ stacks and exposed portions of said lower metallization level;

depositing an interlevel dielectric (ILD) layer over said cap layer; and

defining via openings in said ILD layer, wherein portions of said cap layer atop said lower metallization level are used as an etch stop.

[c8] (previously presented) 8. The method of claim 7, further comprising:

subsequent to defining said via openings, defining openings for said upper metallization level in said ILD layer;

wherein portions of said cap layer atop said MTJ stacks are used as an etch stop.

[c9] (previously presented) 9. The method of claim 8, further comprising:

removing portions of said cap layer exposed by said upper metallization openings and said via openings; and

filling said upper metallization openings and said via openings with a conductive material by dual damascene processing.

[c10] (previously presented) 10. A magnetic random access memory (MRAM) device, comprising:

a magnetic stack layer formed on a lower metallization level, said magnetic stack layer including a non-ferromagnetic layer disposed between a pair of ferromagnetic layers;

a conductive hardmask layer formed over said magnetic stack layer; and

an array of magnetic tunnel junction (MTJ) stacks, said MTJ stacks created by the removal of selected portions of said hardmask layer and said magnetic stack layer, wherein said MTJ stacks including remaining portions of said magnetic stack layer and said hardmask layer, and wherein said hardmask layer forms a self aligning contact between said magnetic stack layer and an upper metallization level formed above said MTJ stacks.

[c11] (previously presented) 11. The MRAM device of claim 10, further comprising:

a cap layer deposited over the MTJ stacks and exposed portions of the lower metallization level;

an interlevel dielectric (ILD) layer deposited over said cap layer; and

a plurality of upper metallization level openings formed in said ILD layer;

wherein portions of said cap layer atop said MTJ stacks are used as an etch stop for said upper metallization openings.

[c12] (previously presented) 12. The MRAM device of claim 11, further comprising:

a plurality of via openings defined in said ILD layer, wherein portions of said cap layer atop said lower metallization level are used as an etch stop for said via openings.

[c13] (previously presented) 13. The MRAM device of claim 12, further

comprising:

a conductive material filled into said upper metallization openings and said via openings, wherein said conductive material contacts lower metallization level and said hardmask layer after removal of portions of said cap layer.

[c14] (previously presented) 14. The MRAM device of claim 10, wherein said hardmask layer comprises a conductive material selected from the group of: tantalum, tungsten, titanium, tantalum nitride, tungsten nitride, titanium nitride, and combinations comprising at least one of the foregoing.

[c15] (previously presented) 15. The MRAM device of claim 11, wherein said cap layer comprises silicon nitride.